

REMARKS

Claims 1 and 3-16 are pending in the application. Claims 1, 3-6, 8-10, 12-14 and 16 are allowed. Claims 7, 11 and 15 are rejected. Claim 7 is hereby amended.

Claims 7, 11 and 15 are rejected under 35 USC § 102 as anticipated by US 5,828,245, Brambilla *et al.*

Applicant respectfully submits that claim 7 is not anticipated by Brambilla *et al* and is allowable. The Examiner asserts that "(Vcap is a continuous function of time) as called for in claim 7". However, Applicant draws the Examiner's attention to the fact that Claim 7 requires generating "a feedback current and said charging current with continuous magnitudes that are progressive functions of said capacitor voltage so that the rate of change of said capacitor voltage is a continuous function of time." (emphasis added). It is clear that the current producing circuit of Brambilla *et al* produces a "ramp" voltage by producing a capacitor voltage Vcap whose rate of change is not a continuous function of time as required by present claim 7 but is a discontinuous function of time, the rate of change dV/dt of the capacitor voltage being alternately 0, $+I/C_{cap}$, $0 -I/C_{cap}$ and again 0, where 'I' is the charging/discharging current I_c or I_d and C_{cap} is the capacitance (see col. 5 lines 6-8). The ramp voltage of Brambilla *et al* is produced by charging and discharging currents which are not continuous, as required by claim 7, but switch between 0, I_c , 0, I_d and again 0.

In this respect, the passage at col. 5 lines 51-58 of Brambilla *et al* reads: "At $t(0)$, there is an off to on command and the op-amp 16 is enabled for operation." ... "After the time delay, t_1 , a full bias command current is applied to the amplifier and the capacitor voltage starts to ramp up" The passage at col. 6 lines 1-2 of Brambilla *et al* reads: "When an on to off command is received at time t_3 , the Vcap starts down." Figure 2 clearly shows an abrupt, discontinuous change of slope - that is to say of the rate of change of the voltage Vcap - at times t_1 , shortly after t_2 , t_3 and t_4 "

The absence of discontinuities in the rate of change of the switched signal in accordance with the invention of present claim 7 avoids generating harmonics of the basic frequency and avoids issues of electromagnetic compatibility that are not avoided nor foreshadowed by Brambilla *et al.* Accordingly it is submitted that claim 7 is not

anticipated nor rendered obvious by Brambilla *et al.* Claim 7 is therefore submitted to be allowable.

Claims 11 and 15 depend on claim 7 and are submitted to be allowable at least for this reason. In addition, claim 11 requires "said capacitor voltage varies substantially as a sinusoidal half-cycle having a single frequency to define said edge of said switched signal". Brambilla *et al.* teaches that the capacitor voltage should vary as a ramp, with discontinuous rates of change (slope) with time, which inherently produces harmonics of the basic frequency and Applicant respectfully submits that this points away from the invention of claim 11.

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

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